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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,768	05/27/2004	Michael P. Chudzik	BUR920030163US1	3767

7590 05/26/2006

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EXAMINER	
ULLAH, ELIAS	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,768	CHUDZIK ET AL.	
	Examiner	Art Unit	
	Elias Ullah	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application filed on 5/27/2004.

Election/Restrictions

Applicant's election without traverse of group I in the reply filed on 5/15/06 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 1, 4, 5, 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanable et al. US 6, 762,107 dated 7/13/2004.

2. Regarding claim 1, 8, Watanable et al. shows a method of fabricating a capacitor, comprising forming a bottom electrode (Fig. 1, 5) ; forming at least one lower surface expansion structure to the bottom electrode (Fig. 1, 2); conformally depositing an insulator film to exposed portions of the bottom electrode and at least one lower surface expansion stricture (Fig. 2, 6); and forming a top electrode (Fig. 2, 7) having a planar surface with at least one upper surface expansion structure (8) separated from the at least one lower surface expansion structure by the insulator film (6).

3. Regarding claim 4, Watanable et al. shows forming lower surface expansion structures in electrical communication with the bottom electrode by forming gaps between lower surface expansion structures; exposing sidewalls of the lower surface expansion structures and portions of the bottom electrode; conformally depositing an insulator film on the portions of the bottom electrode and sidewalls of the multiple lower surface expansion structures; and forming multiple surface expansion structures of the at least one upper surface expansion structure protruding into the gaps and separated the multiple lower surface expansion structures by the insulator film (col. 14, lines 21-45).

4. Regarding claim 5, Watanable et al. shows the multiple lower surface expansion structures are interleaved with the multiple upper surface expansion structures (col. 15, lines 13-20).

5. Regarding claim 7, Watanable et al. shows a second capacitor using the steps of claim 1, and arraigning the second capacitor on a top of the capacitor of claim 1 (col. 15, lines 50-57).

6. Regarding claim 9, Watanable et al. shows the top electrode and the at least one upper surface expansion structures are formed simultaneously (col. 18, lines 44-57).

7. Regarding claim 10, Watanable et al. shows the at least one lower surface expansion structure is formed by depositing an interlayer dielectric material on the bottom electrode (col. 14, lines 25-30); patterning the interlayer dielectric material to form factors; depositing conductor material into the features such that the conductor material is in content with the bottom electrode; further patterning

the interlayer dielectric material to from gaps between the depositing conductor material (col. 16, lines 50-65).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanable et al. in view of An et al. US 6,686,620.

10. As to claim 2, Watanable et al. is applied as above but does not expressly disclose planarizing a surface of the top electrode by a polishing process.

11. As to claim 2, An et al. teaches planarizing a surface of the top electrode by a polishing process (col. 5, lines 30-36). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plain surface by polishing process of Watanable et al. because such process is used as planarizing surface for an electrode.

12. **Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanable et al. in view of Wohlfahrt US 6,720,598.**

13. As to claim 3, Watanable et al. is applied as above but does not expressly disclose the bottom electrode is capacitively coupled to the top electrode.

14. As to claim 3, Wohlfahrt teaches the bottom electrode is capacitively coupled to the top electrode (col. 1, lines 38-45). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically couple two capacitors of Watanable et al. because such process is used to connect between two capacitors.

15. **Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanable et al. in view of Chi et al. US 6,362,012.**

16. As to claim 6, Watanable et al. is applied as above but does not expressly disclose the at least one lower surface expansion structure is a first spiral shape.

17. As to claim 6, Chi et al. teaches the at least one lower surface expansion structure is a first spiral shape (col. 5, lines 29-33). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a surface made of spiral shape of Watanable et al. because such process is used to support for capacitor electrode.

18. **Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanable et al. in view of Radens et al. US 6,794,726.**

19. As to claim 11, Watanable et al. is applied as above but does not expressly disclose the patterning of the interlayer dielectric layer is one of dual tone resist, sidewall image transfer and masking using self-assemble nanocrystals.

20. As to claim 11, Radens et al. teaches the interlayer dielectric layer is one of dual tone resist, sidewall image transfer and masking using self-assemble nanocrystals (col. 5, lines 30-35). In view of this disclosure, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to transfer image by dual tone resist of Watanable et al. because dual tone resist edge patterning process have high quality of image formation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Ullah whose telephone number is 571-272-1415. The examiner can normally be reached on 8-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MICHAEL LEBENTRITT can be reached on (571)272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER

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